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A 1 GHz Integrated Circuit with Carbon Nanotube Interconnects and Silicon Transistors

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ABSTRACT

Due to their excellent electrical properties, metallic carbon nanotubes are promising materials for interconnect wires in future integrated circuits. Simulations have shown that the use of metallic carbon nanotube interconnects could yield more energy efficient and faster integrated circuits. The next step is to build an experimental prototype integrated circuit using carbon nanotube interconnects operating at high speed. Here, we report the fabrication of the first stand-alone integrated circuit combining silicon transistors and individual carbon nanotube interconnect wires on the same chip operating above 1 GHz. In addition to setting a milestone by operating above 1 GHz, this prototype is also a tool to investigate carbon nanotubes on a silicon-based platform at high frequencies, paving the way for future multi-GHz nanoelectronics.

The performances of integrated circuits have been steadily improved over the last few decades through miniaturization of the transistors and the interconnect wires. In addition to shrinking the building blocks, new materials have been progressively introduced in the manufacturing of integrated circuits to further improve their performances. Maintaining this trend of higher-performance integrated circuits into the future will increasingly require the use of materials at the nanoscale. Due to their nanoscale size and outstanding intrinsic electronic properties, carbon nanotubes (CNTs) are promising materials for future nanoelectronics. Semiconducting CNTs are already being researched as the electron channel for nanotransistors.[1,2] Similarly, metallic CNTs have also been proposed as effective wires[3−5] for interconnecting the transistors. In this work, we have built the first integrated circuit combining silicon transistors and CNT interconnect wires on the same chip operating above 1 GHz. This prototype demonstrates that a single carbon nanotube can be effectively used to transmit GHz digital signals in between transistors.

The most advanced integrated circuits consist of several millions (sometimes billions) of transistors, interconnected by kilometers of copper wires within a 1 cm^2 silicon chip. The number of transistors integrated on a single chip is predicted to increase even further,[6] requiring even smaller transistors and narrower copper wires in the future. As copper wires are scaled down, they face two principal issues. First, their electrical resistivity degrades due to increasing electron scattering by the grain boundaries and the wire surface.[7−9] Second, their reliability is becoming a growing concern due to the increasing current density (>2 MA/cm^2) that they need to withstand.[10] A quest for alternative interconnect materials engineered at the nanoscale has thus been initiated to solve these two problems.[11] Metallic CNTs are attractive interconnect materials because they address, in principle, the two problems faced by copper wires. First, due to their 1-D nature, electrons can travel much further than in copper without scattering.[12,13] Second, they can withstand current density greatly exceeding the limit of copper.[14] Another advantage of metallic CNTs as interconnect materials is that they are scalable all the way down to the 1 nm regime.[5] As a result of these attractive attributes, CNTs are actively researched as future interconnect materials in vertical vias[15−17] and horizontal interconnects.[18] However, co-integrating CNT interconnects in the dominant silicon-based CMOS platform remains a challenge.

In fact, there has been no experimental demonstration that a metallic CNT can indeed function as an interconnect wire in an electronic chip and successfully transmit GHz digital signals from one transistor to another. Previous attempts[19,20] to co-integrate silicon transistors and CNTs were limited to the low-frequency regime. Others[21−24] have recently mea-

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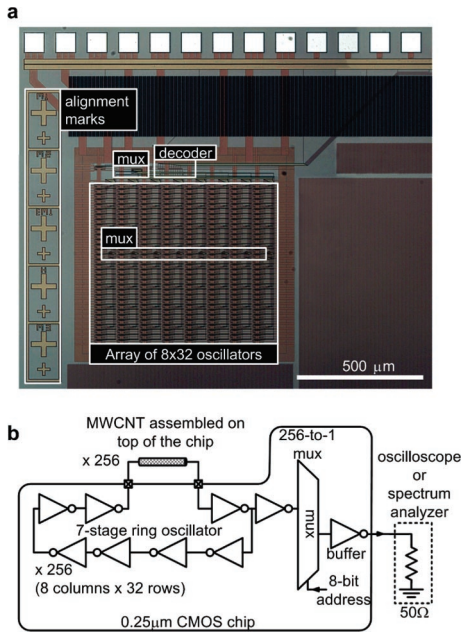

Figure 1. CMOS platform chip before the assembly of the MWCNT interconnects. (a) Chip photograph. (b) Circuit diagram. The chip, which is fabricated in a 0.25 μm CMOS process, contains 256 ring oscillators with an intentionally missing interconnect wire, to be implemented with a MWCNT. In addition, the chip contains selection circuitry (multiplexer: mux, and decoders).

sured the electrical properties of individual CNT interconnects in the radio frequency regime (>1 GHz), but their functionality as an interconnect wire in a working standalone integrated circuit has not been demonstrated.

We address this need in this letter. We designed, fabricated, and tested the first integrated circuit with silicon-based transistors and CNT interconnects operating above 1 GHz. More specifically, we assembled multi-wall CNT (MWCNT) interconnects on top of a CMOS chip fabricated in a 0.25 μm silicon CMOS process containing about 11 000 transistors. The MWCNTs were used as electrical wires interconnecting various stages of conventional ring oscillators. Successful co-integration of silicon transistors and MWCNT interconnects was demonstrated by the correct functionality of the fabricated oscillators.

The CMOS platform chip consisted of an array of 256 ring oscillators and the selection circuitry to select one ring oscillator at a time. The total chip area was 5 mm $\times$ 5 mm, but the circuitry described in this paper only occupied 1/8 of the total area. The chip was fabricated in a 0.25 μm CMOS process. Figure 1 shows the CMOS chip photograph and the circuit diagram. By design, each oscillator was missing one interconnect wire and therefore did not oscillate as it was.

The bare CMOS chip was postprocessed in the clean room of the Stanford Nanofabrication Facility. Growing MWCNTs directly on the CMOS chip was not possible as it would have damaged the CMOS circuitry due to the high temperature required for MWCNT growth (typically >500C). Instead, we used commercially available MWCNTs with an average length around 5 μm and an average diameter around 70 nm. The process flow is illustrated in Figure 2. We first patterned an array of gaps in between gold electrodes. We dispersed the MWCNTs in ethanol. We then applied an alternating electric field to assemble and precisely position the MWCNTs in the gaps between the gold electrodes using the dielectrophoretic effect.[23,25,26] The MWCNTs were then secured in place by metal clamps deposited at both ends of the MWCNTs. Once the MWCNTs were on the chip, via holes were etched through the CMOS passivation layer to reveal the topmost aluminum metal layer of the CMOS chip. The vias were finally filled with titanium, thereby establishing electrical connections between the underlying silicon CMOS transistors and the MWCNT interconnects. Figure 3 shows the chip at the end of the MWCNT assembly process. As the MWCNT interconnects were precisely assembled by dielectrophoresis literally right on top of the silicon transistors, the parasitic capacitances were minimized (<10 fF). This is a key aspect of this work because it allows operation above 1 GHz for the first time.

The postprocessed chip was wire bonded to a pin grid array package and mounted onto a printed circuit board for electrical testing. The oscillation amplitude and frequency were measured with a spectrum analyzer. The 19 oscillators out of 256 (yield ~ 8%, limited by the MWCNT dielectrophoresis assembly) that were properly wired by a MWCNT interconnect did indeed oscillate (Figure 4a,b), demonstrating

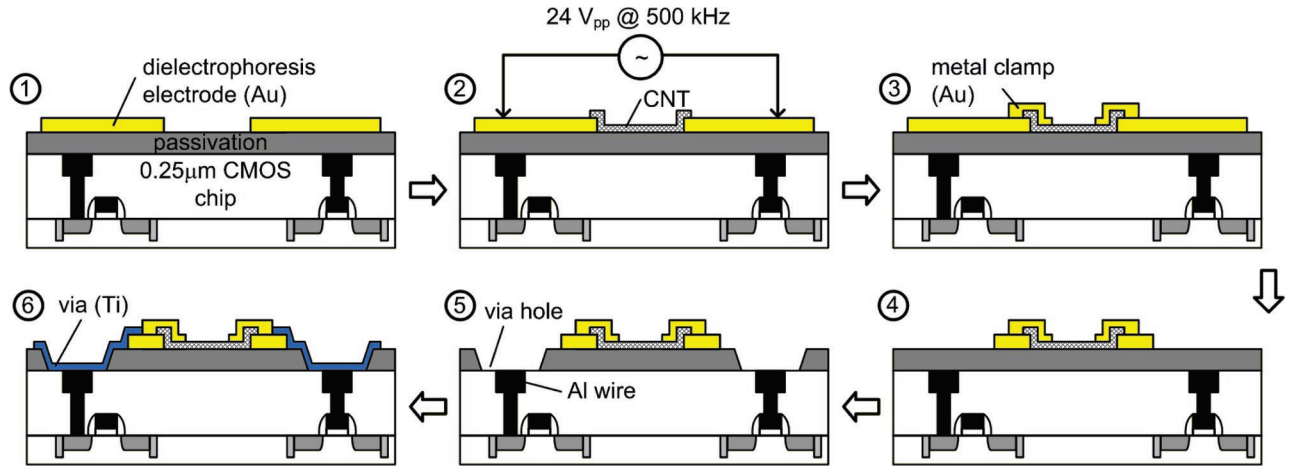

Figure 2. Process flow to assemble an array of MWCNT interconnects on top of a platform CMOS chip.

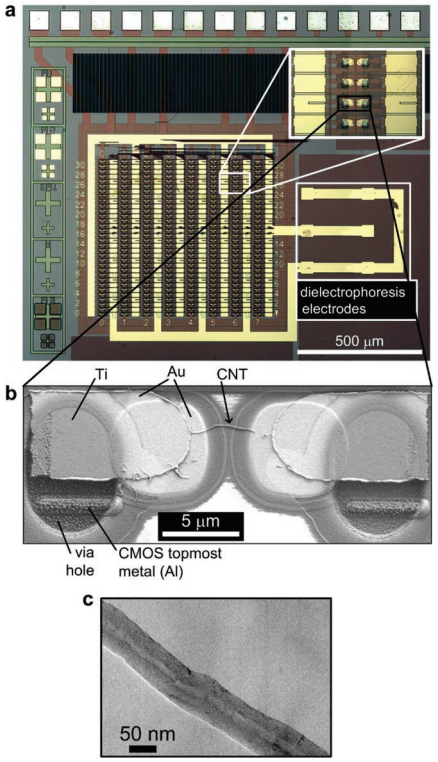

Figure 3. CMOS platform chip after the assembly of the MWCNT interconnects on the chip surface. (a) Chip photograph. (b) Close-up SEM image of one fabricated MWCNT interconnect on top of the chip. The white cloud surrounding the metals in the SEM image is an artifact due to charging of the sample during SEM imaging. (c) TEM image of a typical MWCNT used in this work.

the feasibility of MWCNT interconnects in a silicon environment. The fastest oscillators oscillated at a frequency above 1 GHz, confirming that MWCNT interconnects can successfully transmit GHz signals. All of the assembled MWCNT interconnects had different diameters (from 50 to 100 nm) and different contact geometries. Both of these factors contributed to variations in the resistances of the MWCNT interconnects, which in turn yielded variations in the oscillator frequencies (Figure 4a). The MWCNT interconnect resistance can be inferred from the measured oscillation frequency as follows. Recalling that the oscillation period of a ring oscillator is given by twice the delay around the oscillator loop, half of the oscillation period equals the sum of two delays, the delay through the CMOS stages plus the RC delay contributed by the MWCNT interconnect resistance and the load capacitance driven by the MWCNT. Modeling the MWCNT interconnect as an ideal resistor, we have used HSpice transistor-level circuit simulations to extract the relationship between the MWCNT resistance R_{CNT} and the oscillation period T_{osc} (see Supporting Information)

$$\frac{T_{osc}}{2} = 475\ \text{ps} + R_{CNT}\cdot 5\ \text{fF}$$

Using this equation, we calculated that, for the fastest oscillator operating at 1.02 GHz (T_{osc} = 980 ps), the MWCNT interconnect resistance was around 3 kΩ, consistent with our previous experiments with these MWCNTs.[23] This amounted to a resistivity around 500 $\mu\Omega$-cm, 2 orders

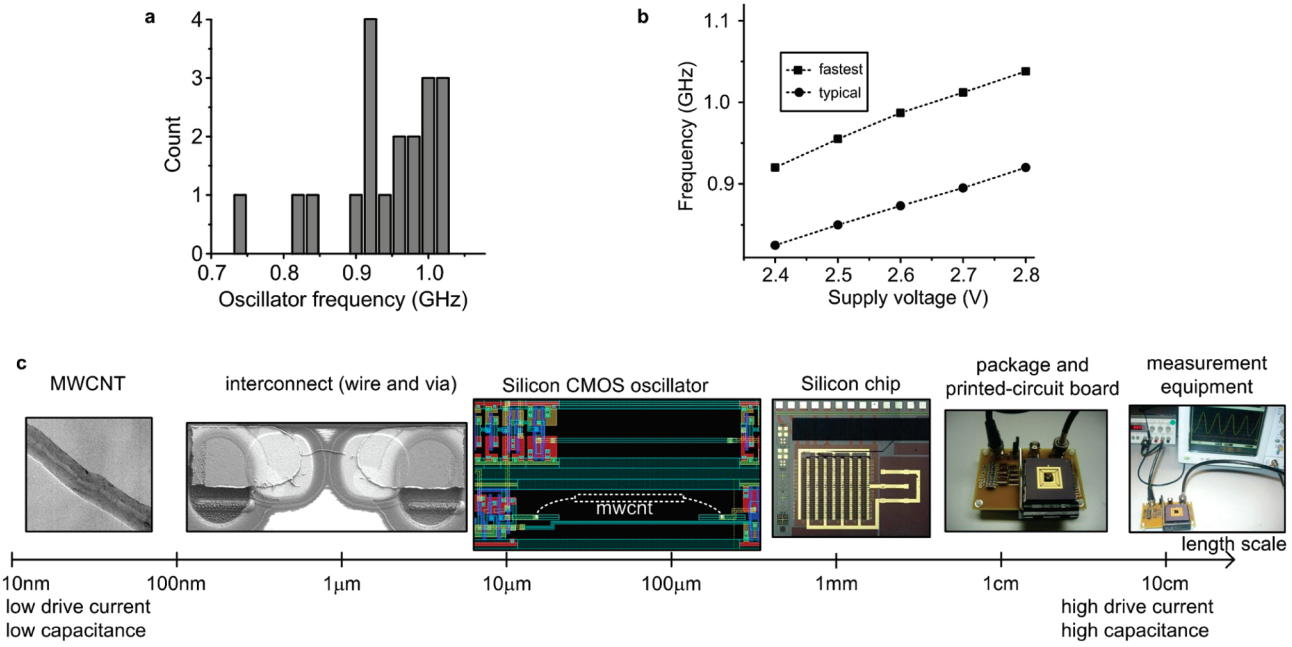

Figure 4. Electrical measurements of the ring oscillators with MWCNT interconnects. (a) Measured oscillation frequency for 19 ring oscillators with MWCNT interconnects at a 2.8 V supply voltage. The oscillators exhibit different oscillation frequencies due to the variability in the assembled MWCNT resistances. The fastest oscillators with MWCNT interconnects operate above 1 GHz at the 2.8 V supply voltage. (b) Measured oscillation frequency as a function of the supply voltage for two particular oscillators, the fastest one (with the lowest MWCNT resistance) and a typical one. (c) Test setup across all of the length scales from the nanoscale MWCNT all the way to the macroscopic measurement equipment. This chain of fast intermediate circuits is the key to achieve GHz operation.

Table 1. Features of the Fabricated Hybrid Integrated Circuit

Silicon CMOS Chip	
technology	0.25 μm CMOS
supply voltage	2.5−2.8 V
number of oscillators	256
number of transistors	11 000
area	2.5 mm × 1 mm
Post-CMOS Assembly of the Carbon Nanotube Interconnects	
number of extra lithography steps	4
carbon nanotube	
type	multi-wall
outer diameter	∼50−100 nm
inner diameter	∼10−20 nm
length	∼5 μm
resistivity	∼500 $\mu\Omega$-cm
voltage applied to assemble the nanotubes	24 V_{pp} @ 500 kHz
nanotube contact metal	gold
via-filling metal	titanium
Completed Silicon-CMOS/carbon Nanotube Hybrid	
number of working oscillators	19
highest oscillation frequency	1.02 GHz

of magnitude higher than the resistivity of copper. This high resistivity can be attributed to the average structural quality and purity (starting material purity: 95%) of our MWCNT materials rather than to a fundamental limitation of MWCNTs. Work is currently underway to improve the resistivity of our MWCNT interconnects and bring it closer to the resistivity of copper. Higher operation frequencies (>1 GHz) could be achieved by using MWCNTs with lower resistivity or faster silicon CMOS circuits or any combination of the two.

In conclusion, we have demonstrated that CNT interconnects can be integrated with silicon CMOS transistors on the same chip. We have also showed, for the first time, that these CNT interconnects can transmit GHz digital signals between transistors. Table 1 summarizes the features of our prototype integrated circuit. The key in achieving GHz operation with individual MWCNT interconnects, and more generally any individual nanoelectronic devices/structures, is to have a chain of fast circuits spanning all length scales from the nanoscale all the way up to the macroscopic test instruments (Figure 4c). Conventional microelectronic circuits in silicon CMOS technology are natural choices in the middle of this chain because they bridge the gap from the microscale to the macroscopic scale. Without this intermediate CMOS link, individual nanoscale devices would not be able to effectively drive any macroscopic circuits at GHz frequencies directly because of their low current drive compared to the macroscopic parasitic capacitances. Our approach opens up the possibility of in situ GHz benchmarking of nanoelectronic devices in a silicon environment.

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Supporting Information Available: Description of materials and methods including MWCNT suspension and deposition, details of the post-CMOS processing steps, electrical test setup, and a figure showing how to extract the relationship between the oscillation frequency and the MWCNT resistance from HSpice circuit simulation. This material is available free of charge via the Internet at http://pubs.acs.org.

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